10 GbE (ETH-MAC-UDP-IP) FPGA IP Core P/N—10GbE-IPCORE-1

Apogee Applied Research, Inc.

- Full Line Rate Packet Processing with packet sizes greater than 1000 bytes
- Subset of 802.3 including: Full Duplex Operation, Receive/Transmit normal frames, Append/Check FCS, Discard Malformed Frames, Append/Remove preamble, SFD and padding, Inter-frame gap enforcement, Unicast/ Multicast, Responds to ARP
- 802.1Q VLAN
- IPv4, RFC 791
- IGMPv2, RFC2236 and works with IGMPv3
- UDP, RFC 768, VITA 49
- MTU sizes up to 1500 octets

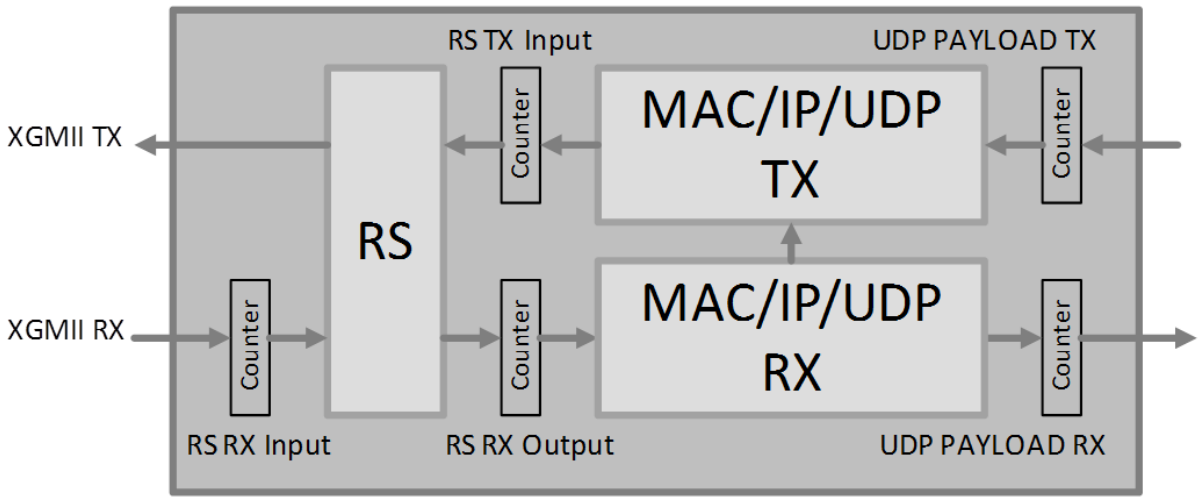
Core Description

The Ethernet processor handles the break-down and analysis of incoming packets and the generation of outgoing packets. It handles the Physical (10GbSFP+), Link (Ethernet, ARP), Internet (IPv4,IGMP), and Transport (UDP) layers. The Ethernet processor uses a dual proprietary microcoded Finite State Machine (FSM) to process the incoming and outgoing packets. The FSMs are connected for handling of automated response packets such as ARP and IGMP. Each FSM contains a large 512 entry table for storage and high-speed search of the possible packet addresses. The address table contains the MAC address, VLAN, IP, and UDP port. The processor supports multicast using IPv4 and IGMPv2 and IGMPv3.

Resource Usage— Compiled in a Virtex-6

Resource type	*Quantity used*
Slices	5151
Registers	6228
LUTS	12470
LUT RAM	2972
Block RAM	19

Block Diagram



Pin-out Description

Pin Name	I/O	Description	CLK MHz
config_clk	in	Configuration Clock	35
config_mem_base_addr [31:0]	In	The base address register offset	config_clk
config_mem_write_en	in	Asserted to enable a write	config_clk
config_mem_write_add [31:0]	in	Contains the write address during a write	config_clk
config_mem_write_data [15:0]	in	Contains the write data during a write	config_clk
config_mem_read_en	in	Asserted to enable a read	config_clk
config_mem_read_addr [31:0]	in	Contains the valid read address while read_en is asserted	config_clk
config_mem_read_data [15:0]	out	After 3 clock cycles, read data is asserted, otherwise = 0	config_clk
proc_clk	in	Processor Clock	90
proc_search_clk	in	LUT Search Clock	250
phy_clk	in	XGMII Physical Layer Clock	156.25
xgmii_tx_data_rising [31:0]	out	XGMII transmit data for rising edge of clock	phy_clk
xgmii_tx_ctrl_rising	out	XGMII transmit control for rising edge of clock	phy_clk
xgmii_tx_data_falling [31:0]	out	XGMII transmit data for falling edge of clock	phy_clk
xgmii_tx_ctrl_falling [3:0]	out	XGMII transmit control for falling edge of clock	phy_clk
xgmii_rx_data_rising [31:0]	in	XGMII receive data for rising edge of clock	phy_clk
xgmii_rx_ctrl_rising [3:0]	in	XGMII receive control for rising edge of clock	phy_clk
xgmii_rx_data_falling [31:0]	in	XGMII receive data for falling edge of clock	phy_clk
xgmii_rx_ctrl_falling [3:0]	in	XGMII receive control for falling edge of clock	phy_clk
udp_payload_tx_data [63:0]	in	64-bit data path containing the payload + mini-header	phy_clk
udp_payload_tx_sof	in	Asserted at the last word of the packet	phy_clk
udp_payload_tx	in	Asserted at the first word of a packet	phy_clk
udp_payload_tx_val	in	Asserted to indicate data is valid	phy_clk
udp_payload_tx_num_bytes [63:0]	in	Number of bytes minus one in the current word(0=1Byte)	phy_clk
udp_payload_tx_rdy	out	Asserted when the interface can accept data	phy_clk
udp_payload_rx_data [63:0]	out	64-bit data path containing the payload + mini-header	phy_clk
udp_payload_rx_sof	out	Asserted at the last word of the packet	phy_clk
udp_payload_rx_eof	out	Asserted at the first word of a packet	phy_clk
udp_payload_rx_val	out	Asserted to indicate data is valid	phy_clk
udp_payload_rx_num_bytes [63:0]	out	Number of bytes minus one in the current word(0=1Byte)	phy_clk

Files—Functional Testing

Source Netlist File: Ethernet_Module.ngc
Simulation File: Ehternet_Module.vhd

Functional Testing
An example VHDL testbench is provided for use in a suitable VHDL simulator. The compilation order of the source code is the same as that outlined in the source file description above.

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Apogee Applied Research, Inc. provides engineering services and hardware systems to commercial and government end users. Our main area of expertise is ultra high bandwidth Software Defined Radios. Apogee systems feature advanced Digital Signal Processing techniques and the ability to process a wide variety of signal types.

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