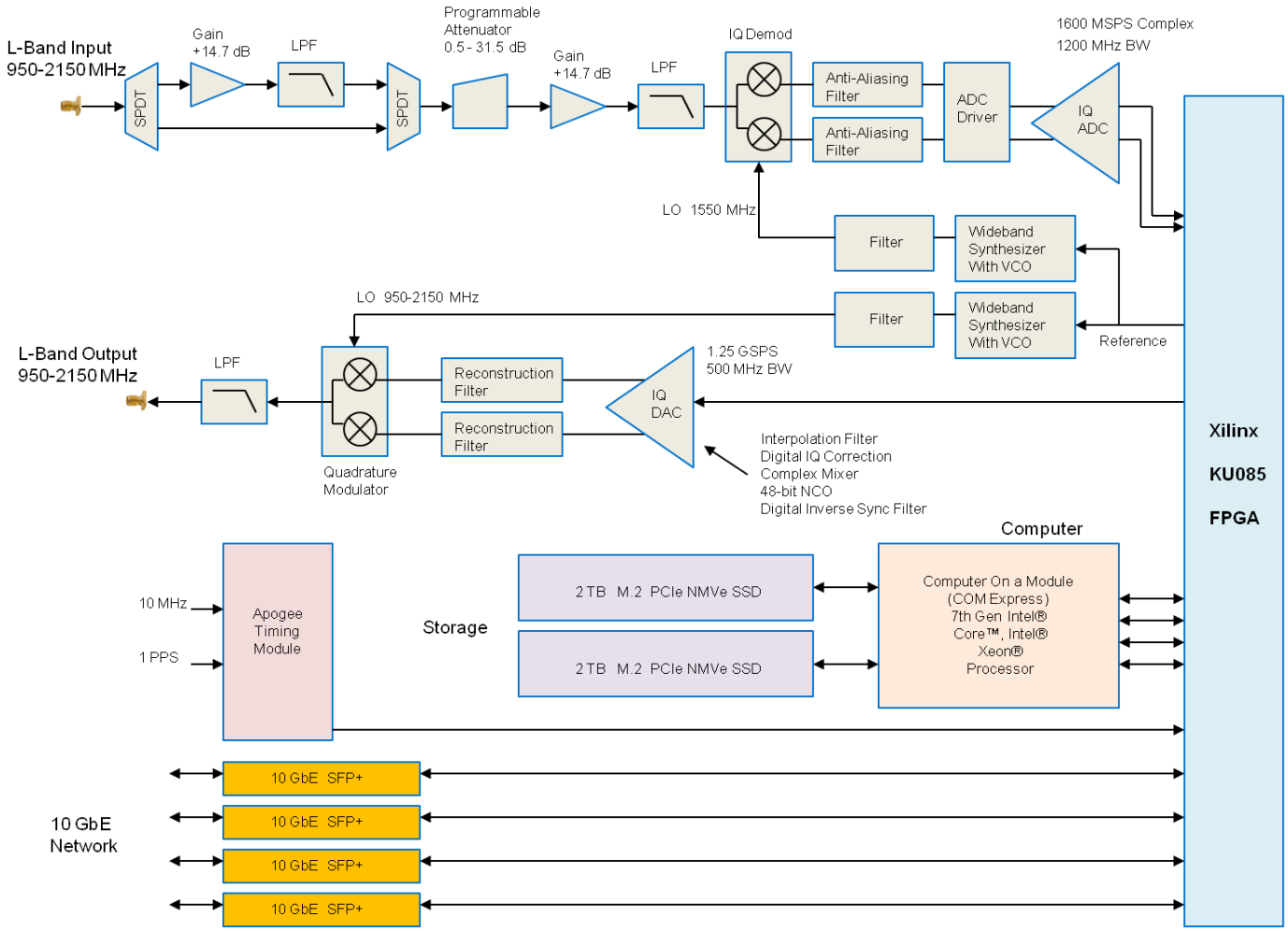
Model 125
L-Band Record and Playback Application

- Record full bandwidth L-Band (1200 MHz BW)
- 10 Minute Record using Internal 4TB Storage
- Add External Storage for longer Record Times
- Loop Mode for Continuous Record
- Tune up to 500 MHz BW Signal from Storage
- Any Tuner Decimation between 2.4 and 32,768
- Stream Tuner Data out via the 10 GbE Ports
- Throttle Tuner Data for Downstream Processors

- Wideband Input Snapshot during Recording
- Playback up to 500 MHz BW
- Playback L-Band Out between 950-2150 MHz
- Playback from Internal Storage
- Playback from External Storage
- Playback from Network Streaming
- VITA-49 Packets with Time Tag (1nsec accuracy)
- Browser Based GUI for Command and Control



Model 125
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Key Specifications— L-band Input and Digitizer

Connector	SMA, 50 Ohm
L-Band Input Frequency Range	950-2150 MHz
Input Power Range, VSWR	-87 dBm to 0 dBm (up to +10 dBM without damage), VSWR ≤ 1.3:1
Gain	14.7dB (selectable), +14.7dB Fixed
Attenuation	Programmable 0.5—31.5 dB
IQ Demod	950-2150 MHz, 1550 MHz LO
ADC Clocking	Internal Wideband Synthesizer with VCO, lockable to Carrier 10 MHz reference
Carrier 10 MHz Reference Requirement	LVDS, 325mV swing
IQ ADC Converter	12-bit, 1.6 GSPS, Texas Instruments—ADC12D1600CIUT
IQ Output Correction	Digital, IP Core provided by Apogee
ADC LVDS Output	LVDS outputs are compatible with IEEE 1596.3-1996
FMC Card Form Factor	ANSI/ VITA 57.1 FPGA Mezzanine Card (FMC), High Pin Count (HPC)
Amplitude Flatness	Uncorrected amplitude ripple over any 80 MHz segment less than ± 0.5 dB Uncorrected amplitude ripple over any 40 MHz segment less than ± 0.3 dB
Out of Band Rejection	Minimum of 50 dB rejection between 0-900 MHz. Minimum of 50 dB rejection between 2200 -3200 MHz.
System Spurious Performance	Typical SFDR of -55 dBc, IMD3 of -57 dBFS Typical
Noise Figure	Typical Noise Figure of 26.9 dB, bypassed input gain Typical Noise Figure of 10 dB with input gain selected
Phase Noise	-78 dBc at 100 Hz. -82 dBC/Hz at 1 kHz. -89 dBC/Hz at 10kHz. -103 dBC/Hz at 100 kHz. -115 dBC/Hz at 1 MHz.

Digital to Analog Converter

Digital to Analog Converter	Texas Instruments— Part Number — DAC3482IRKDT
Resolution, Sample Rate	16-bit, Dual Channel, 1250 MSPS
Data Interface	The DAC3482 has a 16-bit LVDS bus that accepts 16-bit I and Q data in either word-wide or byte-wide formats. In word-wide mode data is sent through a 16-bit bus.
Input FIFO	The DAC3482 includes a 2-channel, 16-bits wide, and 8-samples deep input FIFO which acts as an elastic buffer.
Interpolation	2x to 16x digital interpolation filters with over 90 dB of stop-band rejection
Mixer	Complex mixer allows flexible carrier placement, 32-bit frequency register, 12-bit phase
IQ Offset Correction	Digital Offset, 2s-complement range from –4096 to 4095
Group Delay Correction	DAC3482 has group delay correction block for each DAC channel. The maximum delay ranges from 30 ps to 100 ps.
Quadrature Modulator	Up-convert DAC output to RF frequencies of 950—2150 MHz
Output Power	3-5 dBm typical
Output Frequency Range	L-band, 950 to 2150 MHz
Output Connector	SMA, 50 Ohm

Model 125
L-Band Record and Playback Application

Model 125

Unit Specifications

19 ” 1U rack mount （10 ” depth ）, 0-35C Operating, Humidity 5%—90% Non-condensing, Weight 7.6 lbs

90—264 VAC, 47—63 Hz, Power Factor Corrected