

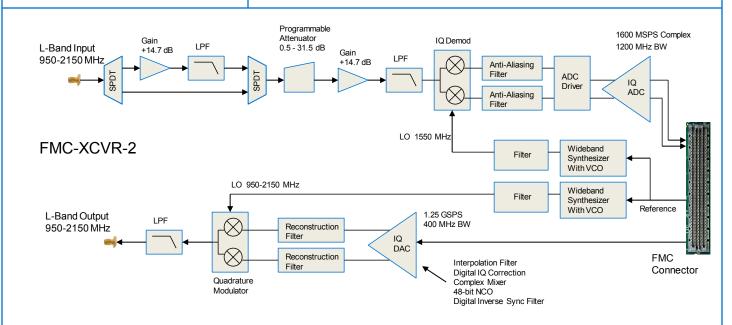
Wideband L-Band Transceiver 1200 MHz ADC BW 400 MHz DAC BW FMC-XCVR-2

- SATCOM
- Software Defined Radio
- Modulation / Demodulation
- Interference Cancelation
- Search and Survey
- Spectral Monitoring

FMC Wideband L-Band Transceiver

The FMC-XCVR-2 uses an analog mixer to center 1200 MHz of the analog L-Band input (950 MHz–2150 MHz input frequency range) at baseband. The 1200 MHz bandwidth is then digitized by a 1.6 GSPS Complex ADC, with the LVDS output routed to the FMC connector.

The FMC-XCVR-2 also features an IQ 16-bit DAC, followed by an IQ modulator to provide up to 400 MHz bandwidth between 950 MHz-2150 MHz. The output center frequency is tunable across the L-Band Output.



Key Specifications— L-band Input and Digitizer

Connector	SMA, 50 Ohm
L-Band Input Frequency Range	950-2150 MHz
Input Power Range, VSWR	-87 dBm to 0 dBm (up to +10 dBM without damage), VSWR \leq 1.3:1
Gain	14.7dB (selectable), +14.7dB Fixed
Attenuation	Programmable 0.5–31.5 dB
IQ Demod	950-2150 MHz, 1550 MHz LO
ADC Clocking	Internal Wideband Synthesizer with VCO, lockable to Carrier 10 MHz reference
Carrier 10 MHz Reference Requirement	LVDS, 325mV swing
IQ ADC Converter	12-bit, 1.6 GSPS, Texas Instruments—ADC12D1600CIUT
IQ Output Correction	Digital, IP Core provided by Apogee
ADC LVDS Output	LVDS outputs are compatible with IEEE 1596.3-1996
FMC Card Form Factor	ANSI/ VITA 57.1 FPGA Mezzanine Card (FMC), High Pin Count (HPC)
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RF Input Chain and Digitizer Performance

Amplitude Flatness	Uncorrected amplitude ripple over any 80 MHz segment less than \pm 0.5 dB
	Uncorrected amplitude ripple over any 40 MHz segment less than \pm 0.3 dB
Out of Band Rejection	Minimum of 50 dB rejection between 0-900 MHz.
	Minimum of 50 dB rejection between 2200 -3200 MHz.
System Spurious Performance	Minimum SFDR of -50 dBc, Minimum IMD3 of -57 dBFS
Noise Figure	Typical Noise Figure of 26.9 dB, bypassed input gain
	Typical Noise Figure of 10 dB with input gain selected
Phase Noise	-78 dBc at 100 Hz.
	-82 dBC/Hz at 1 kHz.
	-89 dBC/Hz at 10kHz.
	-103 dBC/Hz at 100 kHz.
	-115 dBC/Hz at 1 MHz.
System Spurious Performance Noise Figure	Minimum of 50 dB rejection between 2200 -3200 MHz. Minimum SFDR of -50 dBc, Minimum IMD3 of -57 dBFS Typical Noise Figure of 26.9 dB, bypassed input gain Typical Noise Figure of 10 dB with input gain selected -78 dBc at 100 Hz. -82 dBC/Hz at 10 kHz. -89 dBC/Hz at 10 kHz.

Digital to Analog Converter

Digital to Analog Converter	Texas Instruments— Part Number — DAC3482IRKDT
Resolution, Sample Rate	16-bit, Dual Channel, 800 MSPS
Data Interface	The DAC3482 has a 16-bit LVDS bus that accepts 16-bit I and Q data in either word-wide or
	byte-wide formats. In word-wide mode data is sent through a 16-bit bus.
Input FIFO	The DAC3482 includes a 2-channel, 16-bits wide, and 8-samples deep input FIFO which acts
	as an elastic buffer.
Interpolation	2x to 16x digital interpolation filters with over 90 dB of stop-band rejection
Mixer	Complex mixer allows flexible carrier placement, 32-bit frequency register, 12-bit phase
IQ Offset Correction	Digital Offset, 2s-complement range from -4096 to 4095
Group Delay Correction	DAC3482 has group delay correction block for each DAC channel. The maximum delay
	ranges from 30 ps to 100 ps.
Quadrature Modulator	Up-convert DAC output to RF frequencies of 950–2150 MHz
Output Power	3-5 dBm typical
Output Frequency Range	L-band, 950 to 2150 MHz
Output Connector	SMA, 50 Ohm







937-490-2800

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