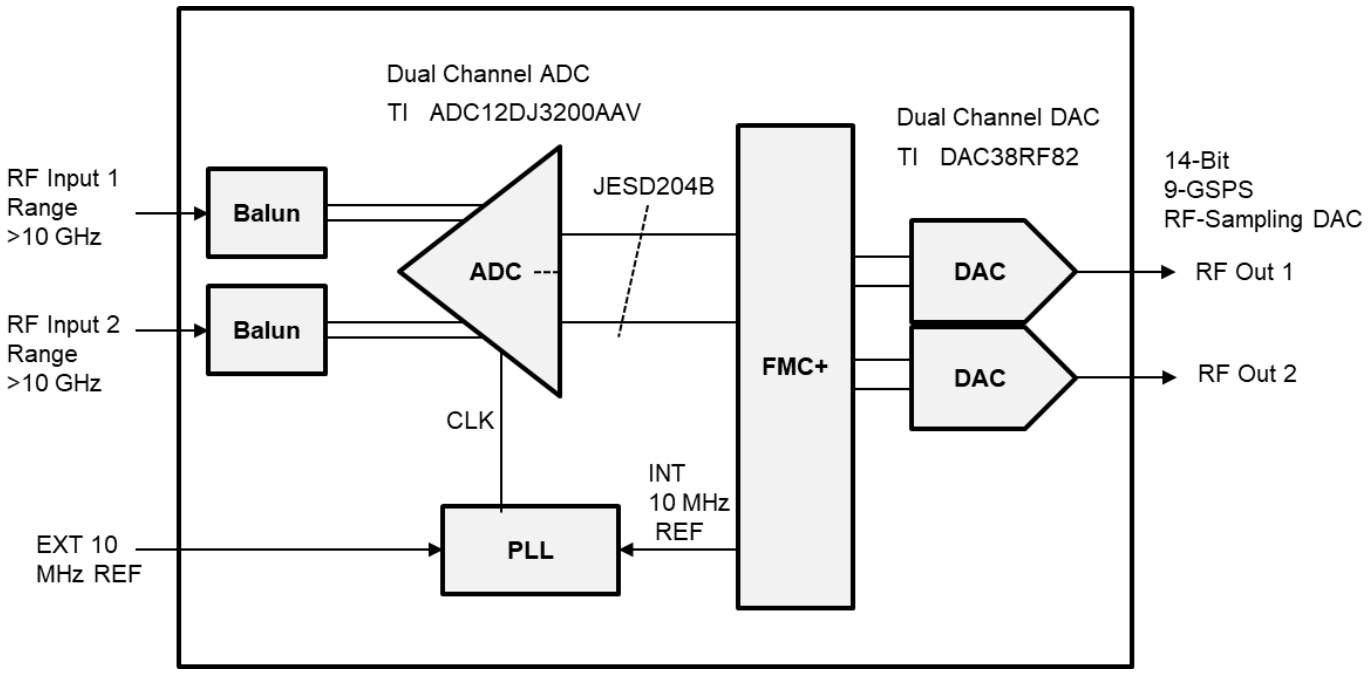
Direct RF Sampling ADC with DAC Converter Module VITA 57.4 FMC+ Form Factor

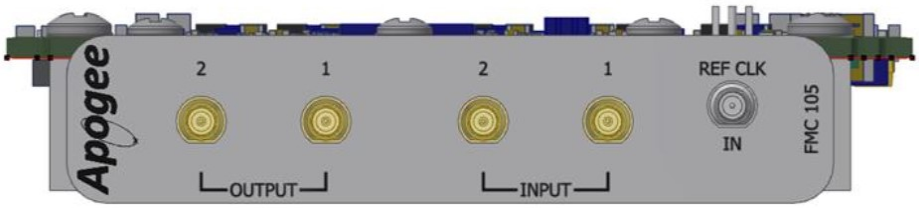
- **SATCOM**
- **Communications (e.g. 5G)**
- **Radar and Electronic Warfare**
- **Communications Test Equipment**
- **Direct RF Synthesis for DOCSIS 3.0/3.1**
- **Microwave Backhaul**

Direct RF Sampling ADC with DAC

Directly sample input frequencies from DC to above 10 GHz. Up to 6.4 GSPS in single channel mode and up to 3.2 GSPS in dual channel mode. Analog input bandwidth (-3dB) is 8.0 GHz (Typ) and the usable input frequency range is >10 GHz. JESD204B output interface.

DAC38RF8x Dual-Channel, Differential-Output, 14-Bit, 9-GSPS, RF-Sampling DAC With JESD204B Interface, On-Chip PLL and Wide-Band Interpolation.





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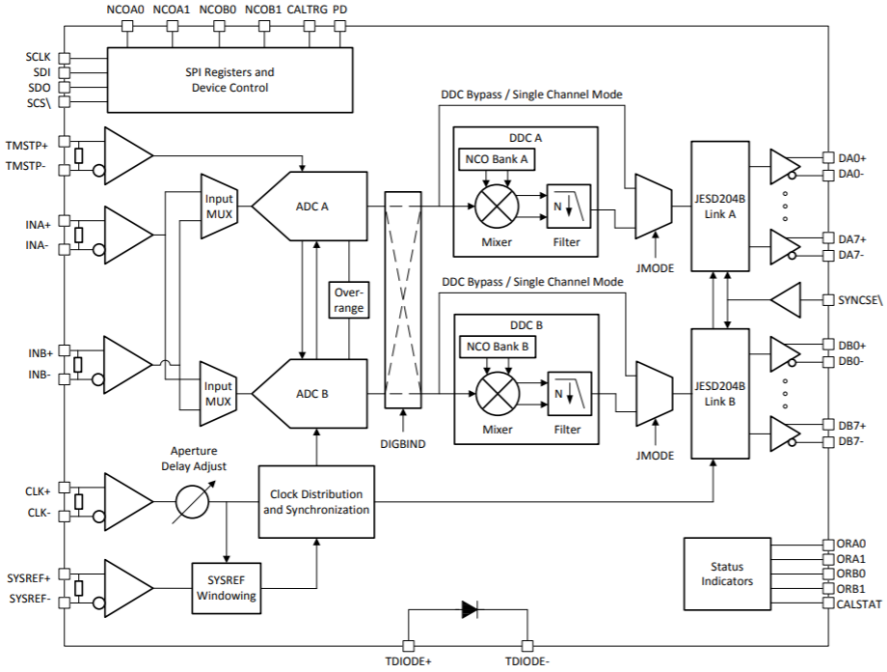

ADC Functional Block Diagram

ADC Specifications (RF parameters are Typical)

Analog-to-Digital (ADC) Part Number.....	Texas Instruments ADC12DJ3200
ADC Resolution.....	12-bits
ADC Sampler Rate.....	Up to 6.4 GSPS Single Channel Mode, Up to 3.2 GSPS Dual Channel Mode
Analog Input Bandwidth.....	8.0 GHz (-3dB)
Usable Input Frequency Range.....	>10 GHz
Noise Floor (No signal, VFS = 1.0 VPP).....	Dual channel mode: -151.8 dBFS/Hz
	Single channel mode: -154.6 dBFS/Hz
Full-scale Input Voltage.....	0.8 Vpp (VFS, default)
JESD204B Serial Data Interface.....	Supports subclass 0 and 1
	Maximum lane rate: 12.8 Gbps
	Up to 16 lanes allows reduced lane rate
DDCs in Dual Channel Mode.....	Real output: DDC bypass or 2x decimation
	Complex output: 4x, 8x or 16x decimation
	Four independent 32-bit NCOs per DDC
RF Input Connector Type.....	SSMC 50 Ohm
Form Factor.....	VITA 57.4 FMC+
Ordering Part Numbers.....	FMC-105-1

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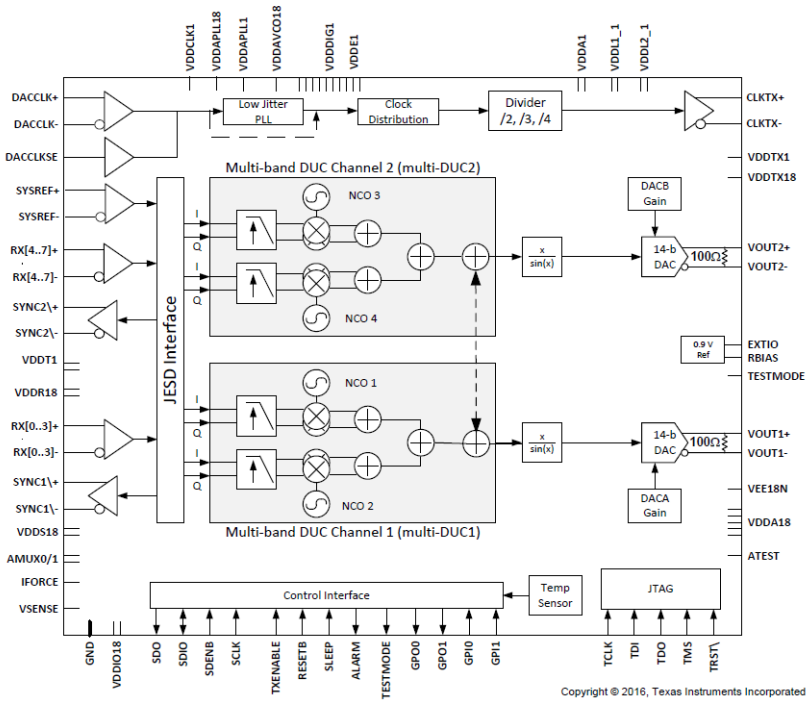

DAC Functional Block Diagram

DAC Specifications (RF parameters are Typical)

- 14-Bit Resolution, 9-GSPS DAC with Multimode Operation
  - 16-Bit, Dual-Channel Data Mode
    - Max Input Rate: 2.5-GSPS
    - Wideband Digital Up-converter
      - Interpolation: 1,2,4,6,8,10,12,16,18,20,24x
  - 12-Bit, Dual-Channel Data Mode
    - Max Input Rate: 3.33-GSPS
    - Wideband Digital Up-converter
      - Interpolation: 1,2,24x
  - 8-Bit, Single-Channel Data Mode
    - Max Input Rate: 9-GSPS
- JESD204B Interface
  - Subclass 1 for Multichip Synchronization
  - Maximum Lane Rate: 12.5 Gbps
- Differential Output
  - Supports DC Coupling
  - RF Full-Scale Output Power (with 2:1 Balun): 3 dBm at 2.14 GHz
- Internal PLL and VCO with bypass
  - DAC38RF82: $f_{C(VCO)}$ = 5.9 or 8.9 GHz
  - DAC38RF89: $f_{C(VCO)}$ = 5 or 7.5 GHz

In dual channel operation, the input interface is capable of data rates up to 3.33 GSPS at 12-bits and 2.5 GSPS at 16-bits resolution without interpolation. When used as a complex baseband transmitter with interpolation modes from 2x to 24x, the DAC38RF82 or DAC38RF89 is capable of synthesizing wideband signals up to 2 GHz bandwidth with 16-bit input resolution and 2.66 GHz bandwidth with 12-bit input resolution.

The 8-bit mode allows an input at the full 9 GSPS maximum DAC sample rate and can synthesize wideband signals from 0 to 4.5 GHz.