Apogee
Applied Research, Inc.

FPGA IP CORES

10Gb/s and 1Gb/s Ethernet Cores

The Ethernet processor handles the break-down and analysis of incoming packets and the generation of outgoing packets. It handles the Physical (10Gb or 1Gb SFP+), Link (Ethernet, ARP), Internet (IPv4,IGMP), and Transport (UDP) layers (TCP/IP also available). The Ethernet processor uses a dual proprietary microcoded Finite State Machine(FSM) to process the incoming and outgoing packets. The FSMs are connected for handling of automated response packets such as ARP and IGMP. Each FSM contains a large 512 entry table for storage and high-speed search of the possible packet addresses. The address table contains the MAC address, VLAN, IP, and UDP port. The processor supports multicast using IPv4 and IGMPv2 and IGMPv3.

Supports:

- Full Line Rate Packet Processing with packet sizes greater than 1000 bytes
- Subset of 802.3 including: Full Duplex Operation, Receive/Transmit normal frames, Append/Check FCS, Discard Malformed Frames, Append/Remove preamble, SFD and padding, Interframe gap enforcement, Unicast/Multicast, Responds to ARP
- 802.1Q VLAN
- IPv4, RFC 791
- IGMPv2, RFC2236 and works with IGMPv3
- UDP, RFC 768, VITA 49
- MTU sizes up to 1500 octets

SDR Packet Processor Core

The SDR Application Layer Packet Processor processes incoming and outgoing Software Defined Radio packets. The App Processor utilizes Apogee's Finite State Machine (ApoFSM) packet processor to quickly process 512-channels of inbound and outbound packet headers. The processor operates on the application layer (Internet Protocol Suite Model) of the packet. It currently supports formats such as SDDS, and is architected to support VITA 49. The processor is designed to interface with the aurora modules.

With the incoming packets the processor handles interpreting and removing the packet header, storing timecode and frequency information in a local memory, and presenting the packet payload and format information to downstream processing. On the transmit side the outgoing packets are received as formatted payloads with a timecode offset value and sideband formatting information. The App Processor then calculates the new timecode based on the received sample offset and timecode memory address values.

There are also two modules, an unformatter and formatter that are used to break the data into samples and put samples back into a payload format. The unformatter receives the packet payload and sideband formatting information. The information is then used to break the payload into data samples that are then sent downstream. The sideband information contains minimum information to unpack the data. The formatter does just the opposite in formatting the data samples into a packet payload. The unformatter and formatter are separate modules that can be instantiated or left out depending on the requirements of the processing.

Parameter	Value
Formats	SDDS/VITA49
App Processing Clock Rate	~90MHz
Interface Clock Rate	156.25MHz in Xilinx Virtex6 w/ -2 speed grade
Unformatter Processing Clock Rate	300MHz(Typical)
Formatter Processing Clock Rate	300MHz(Typical)
Formatter Memory Clock Rate	175MHz(when QDR is 350MHz)
Channels Per App Processor	512
Channels Per Unformatter	1(Typical)/512(Max.)
Channels Per Formatter	512 Per Interface/1024(Total)

Multi-Channel Over-clocked High Speed Real-to-Complex Core

The Real-to-Complex Core converts up to 64-channels of real signal data into complex baseband signals all the while maintaining 80% band-widths. The input is 4 samples wide to support up to 4 times the processing clock frequency. The inputs also support complex data at up to 2x the rate for selectable pass through. The inputs are 16-bit twos-complement. Each sample maintains a channel number to delineate between different streams. There are no restrictions on the order of channels coming into the core. The inputs are gated with a input valid signal so the input data can be at any sample rate less than or equal to than 4 times the processing clock.

- The core also supports timestamp compensation for maintaining very accurate timecode information. It maintains Tperiod/2^18 secs resolution.
- The outputs are 2 complex samples wide with a data valid.
- The configuration is handled by a 32-bit memory mapped interface.
- Selectable direction of shift for Fs/4 shift
- Filter and decimate by 2
- 64-channels per core
- Up to 16-bit Inputs
- 4x real or 2x complex
- Selectable bypass to allow complex inputs on the same port as the real inputs
- Tested Fclk @ 300MHz in Xilinx Virtex6 w/ -2 speed grade
- 4x input for wide band ADC converters (E.g. 4*300MHz = 1200MSPS)
- 2x output to maintain large bandwidths
- -92dBc In-band Aliasing performance

Packet Switch Core

The Packet Switching core routes packets from sources to destinations. Each source and destination handles up to 512-channels. Packet sizes can be between 1 and 1500 Bytes (Inquire about larger sizes). The packet switches handles fanout to multiple destination ports but not multiple channels on the same port. It currently supports 1100MB/s transfer rates per port. The switch contains minimal buffering reduce the logic requirements.   The packets are routed based on the source port and a 9-bit channel field in a 64-bit header on each packet. Packets are routed using a channel number, there is no PHY, High Level IP, or MAC address switching.

- 512-Channels Per Input and Output
- 64-bit paths
- Typical Fclk @ 156.25MHz in Xilinx Virtex6 w/ -2 speed grade
- Max. bandwidth 1250Mbytes/sec (including 64-bit header)
- Max. Packet Size 1500 bytes in increments of 1 byte
- Buffered Inputs
- Fan out to Multiple Outputs supported
- Configurable number of Inputs and Outputs

Contact Apogee Applied Research, Inc. to request detailed IP Core Data Sheets

Multi channel CIC filter Core w/ Roll-off Compensation, Variable Output Bandwidth Filter

The Cascaded integrator-comb (CIC) filter is an efficient implementation of a decimating filter. The filter has dual independent inputs, each with 32-channels. The inputs support individual channel sample rates up to Fclk/6, and aggregate sample rates up to 2 times the processing clock frequency. The input handles 16-bit, twos-complement data. The CIC filter rolloff is compensated internally.

The output bandwidth can be selected, on a per channel basis, in 5% increments from 5% to 80% which allows for significant reduction in filter requirements in downstream processing such as arbitrary resamplers in rate tracking loops.

- The core also supports timestamp compensation for maintaining very accurate timecode information. It maintains $Tperiod/2^{18}$ secs resolution.

- The outputs are 2 complex samples wide with a data valid.

- The configuration is handle by a 32-bit memory mapped interface.

- 64-channels per filter

- Dual 32-Channel 2x Inputs

- 32 channels per input

- Up to 16-bit I/Q inputs

- Per input max. sample rate = Fclk

- Per channel max. sample rate = Fclk/6

- Decimations from 8 to 2048

- Single 64 channel Output 16-bit I/Q

- Output bandwidth independently selectable in 5% increments

- Tested Fclk @ 300MHz in -2 speed grade V6

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Interpolating Resampler

- Single Channel, performs a variable fractional rate interpolation on the input signal

- Output rate is always module clock rate

- Interpolation range from 1.5625 to 200; 2^-17 phase step

- 32 bit control word (fractional interval).   U_ctrl = (fsin/fclk)*2^31   (fractional interval)

- Modified Farrow Architecture (16 polynomials that are 5th order)

- Filter characteristic scales with rate change

- 16-bit complex input 18-bit complex output

- Capable of running in excess of 300 MHz in Xilinx V6-2

- DSP48E1=106, FFs=2919, LUTs=4079

- Stock filter shape ensures 70 dB dynamic range, for specific requirements filter shape can be modified
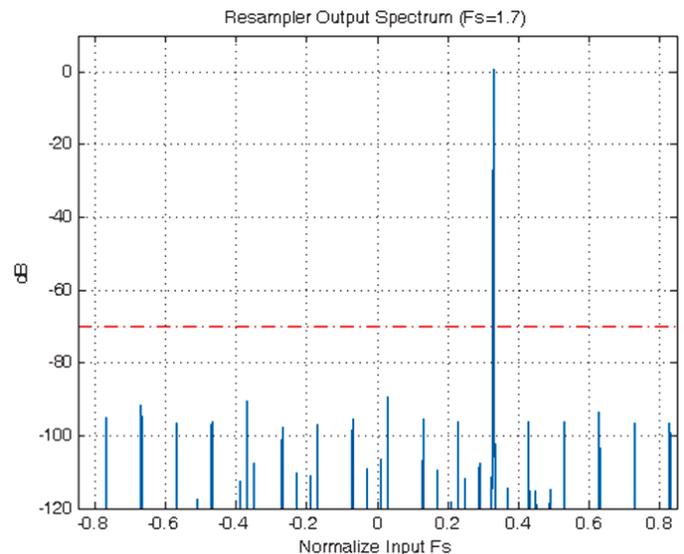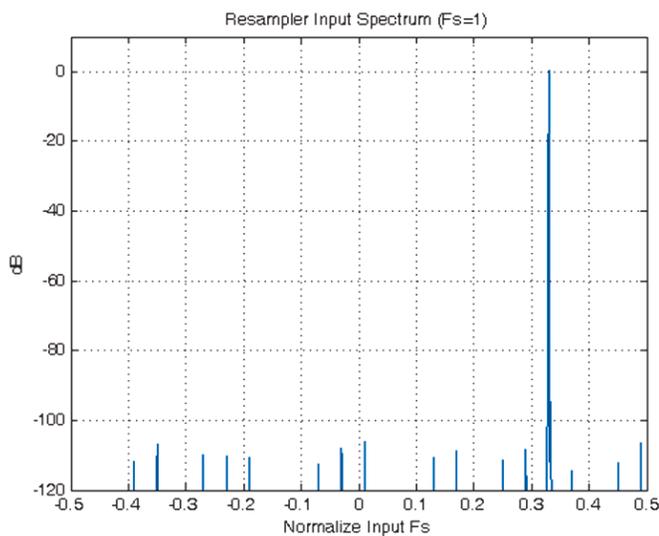
Resampler Input Spectrum (Fs=1)

Resampler Output Spectrum (Fs=1.7)

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Apogee Applied Research, Inc. provides engineering services and hardware systems to commercial and government end users. Our main area of expertise is ultra high bandwidth Software Defined Radios. Apogee systems feature advanced Digital Signal Processing techniques and the ability to process a wide variety of signal types.

Our leadership team has over 45 years combined experience in the field of Digital Signal Processing, and a reputation for outstanding customer service long after the sale. We have a proven track record of delivering systems on time and exceeding customer expectations from concept to delivery.

Apogee's Dayton Facility

- **Engineering**
- **Laboratories**
- **Production**
- **Test**